WHAT IS CLAIMED IS:

1. A multi-level interconnect structure for a semiconductor integrated circuit chip on a semiconductor substrate comprising:

a plurality of electrically conductive metallization levels, each of said metallization levels comprising a plurality of electrically conductive interconnect segments;

a plurality of electrically conductive plugs for electrically connecting between various metallization levels and between said metallization levels and a plurality of semiconductor devices;

a free-space medium occupying at least a substantial portion of the electrically insulating regions within said multi-level interconnect structure; and

an electrically insulating top passivation overlayer for hermetic sealing of said multi-level interconnect structure and for protection of said integrated circuit chip, said top passivation overlayer also serving as a heat transfer medium for facilitating heat removal from said interconnect structure and providing additional mechanical support for said interconnect structure through contact with the top metallization level of said multi-level interconnect structure.

2. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive interconnect segments is made of copper.

3. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive plugs is made of copper.

4. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive interconnect segments and plugs is made of a material comprising silver or aluminum.

5. The multi-level interconnect structure of Claim 1 wherein at least a portion of said electrically conductive interconnect segments and plugs is made of a material comprising a superconducting material.

6. The multi-level interconnect structure of Claim 1 wherein said semiconductor substrate is silicon, or silicon-on-insulator, or galium arsenide.

7. The multi-level interconnect structure of Claim 1 wherein said electrically insulating top passivation overlayer is made of a material comprising silicon nitride, silicon oxynitride, aluminum nitride, diamond-like coating, boron nitride or silicon carbide.

8. The multi-level interconnect structure of Claim 1 wherein said electrically insulating top passivation overlayer comprises a material layer with a plurality of open bonding pad windows and closed resealed windows, the latter used for formation of said free-space medium and subsequent hermetic sealing of said interconnect structure.

9. The multi-level interconnect structure of Claim 1 wherein said multi-level interconnect structure is further supported by an electrically insulating bottom buffer layer, said electrically insulating bottom buffer layer separating said multi-level interconnect structure from underlying transistors and isolation regions fabricated within said semiconductor integrated circuit chip substrate.

10. The multi-level interconnect structure of Claim 9 wherein said top passivation overlayer provides openings to expose the electrically conductive bonding pads and said electrically insulating bottom buffer layer provides openings for electrical connections between a portion of said electrically conductive plugs and said underlying transition within said semiconductor substrate.

11. The multi-level interconnect structure of Claim 9 wherein said multi-level interconnect structure provides mechanical stability through a plurality of interconnections among said electrically conductive interconnect segments and plugs, binding connections between said top passivation overlayer and a portion of the top metallization level, as well as binding connections between a portion of said electrically conductive plugs and said electrically insulating bottom buffer layer.

12. The multi-level interconnect structure of Claim 9 wherein said plurality of electrically conductive levels and plugs is embedded within a sealed cavity formed between said top passivation overlayer and said electrically bottom

buffer layer in conjunction with a free-space dielectric medium.

13. The multi-level interconnect structure of Claim 9, wherein said electrically insulating bottom buffer layer is made of a material comprising silicon nitride, aluminum nitride, diamond-like coating, silicon carbide, or boron nitride.

14. The multi-level interconnect structure of Claim 9, wherein said electrically insulating bottom buffer layer provides additional mechanical support for said multi-level interconnect structure.

15. The multi-level interconnect structure of Claim 14, wherein said electrically insulating bottom buffer layer further provides a blocking material with effective diffusion barrier properties against contamination of said semiconductor substrate by the metallization materials and ionic contaminants.

16. The multi-level interconnect structure of Claim 14 wherein said electrically insulating bottom buffer layer enables formation of said free-space medium without damage to said underlying transitory and isolation regions.

17. The multi-level interconnect structure of Claim 1, wherein said hermetically sealed free-space medium comprises a gaseous material.

18. The multi-level interconnect structure of Claim 1, wherein said hermetically sealed free-space medium comprises vacuum.

19. The multi-level interconnect structure of Claim 17, wherein said gaseous material is in the pressure range of less than 5 atmospheres.

20. The multi-level interconnect structure of Claim 17, wherein said gaseous material is at or near the atmospheric pressure.

21. The multi-level interconnect structure of Claim 17, wherein said gaseous material comprises a high-thermal-conductivity inert gas.

22. The multi-level interconnect structure of Claim 21, wherein said inert gas comprises helium or argon.

23. The multi-level interconnect structure of Claim 17, wherein said gaseous material comprises nitrogen or hydrogen.

24. The multi-level interconnect structure of Claim 17, wherein said gaseous material suppresses electrical leakage currents and gas breakdown within said free-space medium due to said electrically conductive interconnect segments and plugs.

25. The multi-level interconnect structure of Claim 19 wherein the exposed surfaces of said plurality of electrically conductive interconnect segments and plugs further comprise an encapsulation coating layer.

26. The multi-level interconnect structure of Claim 11, wherein said encapsulation coating layer comprises an electrically conductive material (such as TiN_x, TaN_x, Wn_x, or silver).

27. The multi-level interconnect structure of Claim 25, wherein said encapsulation coating layer comprises an electrically insulating material (such as silicon dioxide, silicon nitride, aluminum nitride, aluminum oxide, or diamond-like carbon).

28. The multi-level interconnect structure of Claim 27, wherein said electrically insulating encapsulation coating layer suppresses electrical leakage and breakdown within said interconnect structure.

29. The multi-level interconnect structure of Claim 1 wherein at least a portion of said plurality of electrically conductive interconnect segments and plugs comprises a high electrical conductivity material (such as copper, silver, gold, or a superconducting material).

30. The multi-level interconnect structure of Claim 1, wherein a portion of said electrically conductive plugs comprises the conductive contact plugs which provide electrical connection between the first metallization level and underlying semiconductor devices and are encapsulated

in a conductive diffusion barrier layer (such as TiN_x, TaN_x, Wn_x, Ta, or a ternary conductive barrier material).

31. The multi-level interconnect structure of Claim 30, wherein the plurality of metallization levels between the second level and the top level as well as the plurality of electrically conductive via plugs providing interlevel connections above first metallization level do not utilize any electrically conductive diffusion barrier layers.

32. The multi-level interconnect structure of Claim 9, wherein said top passivation overlayer and said bottom electrically insulating buffer layer are formed using at least one etch-resistant electrically insulating material (such as one or a combination of silicon nitride, aluminum nitride, silicon carbide, boron nitride, or diamond-like coating).

33. The multi-level interconnect structure of Claim 9, wherein said top passivation overlayer and said bottom electrically insulating buffer layer join together to make a sealed contact at the peripheral region of said semiconductor integrated circuit chip to form a hermetically-sealed and mechanically stable cavity encapsulating said plurality of electrically conducting metallization levels, said plurality of electrically conductive plugs, and said free-space medium.

34. The multi-level interconnect structure of Claim 1, wherein at least a substantial portion of contact interfaces among said electrically conductive metallization levels and electrically conductive plugs comprise direct

connections of identical metallization materials without any interfacial contact barrier layers.

35. The multi-level interconnect structure of Claim 1, wherein a plurality of dummy plugs connected to bottom surface of the top passivation overlayer provides additional structural and mechanical support for said multi-level interconnect structure.

36. A method for formation of a multi-level interconnect structure comprising the steps of:

fabricating a plurality of metallization levels, said metallization levels separated by and embedded within a disposable interlevel and inter-metal material layers;

fabricating a plurality of electrically conductive plugs in conjunction with said metallization levels and embedded within said disposable interlevel and inter-metal material layers;

depositing a top insulator layer over said plurality of metallization levels;

forming a plurality of openings within said top insulating layer;

selectively removing said disposable inter-level and inter-metal material layers to form a free-space dielectric medium surrounding at least a substantial portion of said plurality of metallization levels and said electrically a conductive plugs;

forming a hermetically-sealed interconnect structure with a free-space dielectric medium by depositing an electrically insulating material layer and sealing said plurality of openings without substantially shrinking the overall volume of said free-space dielectric medium; and

forming the bonding pad openings.

37. The method of Claim 36, wherein at least a portion of said plurality of metallization levels and electrically conductive plugs is formed within said disposable material layers using a damascene process flow.

38. The method of Claim 36 wherein said multi-level interconnect structure is formed using 2N+1 microlithography masking steps for N metallization levels.

39. The method of Claim 36 wherein said multi-level interconnect structure is formed using 2N+2 microlithography masking steps for N metallization levels.

40. The method of Claim 36 wherein said disposable inter-level and inter-metal material layers comprise silicon oxide.

41. The method of Claim 36, further comprising the step of forming said multi-level interconnect structure to be supported by a bottom electrically insulating buffer layer, said electrically insulating bottom buffer layer separating said multi-level interconnect structure from underlying transistors and isolation regions fabricated within said semiconductor integrated circuit substrate.

42. The method of Claim 36, further comprising the step of forming said electrically insulating bottom buffer layer to provide additional mechanical support for said multi-level interconnect structure.

43. The method of Claim 42, further comprising the step of forming said electrically insulating bottom buffer layer to further provide a dielectric material with effective diffusion barrier properties against contamination of the semiconductor substrate by the contaminating metallization materials and external ionic contaminants.

44. The method of Claim 36, further comprising the step of forming said hermetically-sealed free-space medium to comprise a gaseous material.

45. The method of Claim 44, further comprising the step of forming said gaseous material to be in the pressure range of less than 5 atmospheres.

46. The method of Claim 45, further comprising the step of forming said gaseous material to be at or near atmospheric pressure.

47. The method of Claim 36, further comprising the step of forming said encapsulating layer to comprise an electrically insulating layer.

48. The method of Claim 36, further comprising the step of forming at least a portion of said plurality of electrically conductive interconnect segments and plugs to comprise a high electrical conductivity material.

49. The method of Claim 48 wherein said high electrical conductivity material comprises copper, silver, gold, aluminum, or a superconducting material.

50. The method of Claim 48 wherein said high electrical conductivity material is deposited using chemical-vapor deposition, physical-vapor deposition, and/or electroplating.